Abstract of the Disclosure

A pair of nonvolatile memory transistor are carved from a single polysilicon floating gate on an insulated substrate. After surrounding the poly floating gate with insulator, the poly is etched except for two remnants remaining on lateral sides of the original floating gate. These remnants become a pair of new floating gates for the transistor pair. Prior to etching of the poly, the poly may be used for self-aligned placement of highly doped regions that serve as electrodes for the two transistors. If the single poly floating gate has a minimum feature size for a manufacturing process, the pair of poly remnants remaining after etching are even smaller, perhaps less than a fraction of the minimum feature size. With this small size, the devices will operate by band-to-band tunneling, i.e. without tunnel oxide, characteristic of larger EEPROM and EPROM devices. A single conductive control electrode over the poly remnants can allow both transistors to operate as independent storage devices if bit lines, connected to other electrodes, are phased.